D0 Muon Readout Electronics Design

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Abstract

The readout electronics designed for the D0 Muon Upgrade [1] are described. These electronics serve three detector subsystems and one trigger system. The front-ends and readout hardware are synchronized by means of timing signals broadcast from the D0 Trigger Framework. The front-end electronics have continuously running digitizers and two levels of buffering resulting in nearly deadtimeless operation. The raw data is corrected and formatted by 16-bit fixed point DSP processors. These processors also perform control of the data buffering. The data transfer from the front-end electronics located on the detector platform is performed by serial links running at 160 Mbit/s. The design and test results of the subsystem readout electronics and system interface are discussed.

I. Introduction

Since the previous publication two years ago [2] several aspects of the design have been worked out and tested. The electronics for the muon system now includes 9,500 channels for proportional drift tubes (PDT), 6,000 channels for various types of scintillation counters, and 48,000 channels for mini-drift tubes [3]. A major goal was to develop a unified strategy for readout for all the detector subsystems.

All subsystems that can form a trigger send trigger data to the Trigger Framework (TFW) which is the source of all trigger decisions. These decisions are made on two levels based on inputs from the Level 1 (L1) and Level 2 (L2) trigger systems. The L1 trigger systems generate trigger information synchronously with the beam crossings while the L2 systems operate asynchronously and have an indeterminate decision time within some limit (A third level of trigger is a software filter using complete event information whose decisions are independent of the TFW). The Fermilab accelerator, running in the collider mode, uses the Tevatron RF frequency of 53.104 MHz to synchronize colliding beams. A clock frequency derived from the Tevatron RF divided by seven is used to synchronize the beam crossings within the accelerator. This frequency is the basic frequency for transferring L1 trigger information to and trigger decisions from the Trigger Framework (TFW).

All the muon subsystem front-ends use a strategy of continuously running digitizers for time and charge measurements. The digitizer outputs are connected to digital delays providing the necessary delay for the event data before a trigger decision is returned. Upon arrival from the TFW of an L1 accept decision, data is transferred to the first level of buffering. Both digitizer and delays run synchronously with the Tevatron RF.

The front ends are globally synchronized to the beam crossings and each other by the TFW. It distributes timing and control signals including a copy of the Tevatron RF, L1 and L2 decisions and trigger numbers to the front-end electronics near the detector via the Geographic Sectors (GS) located in the movable counting house. These numbers are used to identify the beam crossing corresponding to the trigger decision and must be consistent across the detector.

II. Muon System

A. Muon Detector Front-End Subsystems

The PDTs (9,500 channels total) have up to 96 wires per chamber. Attached to these chambers are three 32-channel Front-End-Boards (FEB) and one Control Board (CB). The FEBs digitize the time of arrival of the wire signal and the charge of the pad electrodes. The digital delays and L1 buffers are also located on this board. Each FEB is connected to the CB via an 18 bit bi-directional data bus. The CB has a readout controller which fetches data sequentially from each L1 FIFO upon receiving an L1 accept and stores it in DSP memory.

The scintillation counter subsystem (6,000 channels total) includes 48-channel 9U VME scintillator front end cards (SFE). These cards measure arrival time of the scintillation counter signals. There are three charge integrators and ADCs each of which can be attached to a particular channel for use as a photomultiplier gain monitor. Since the gain of a particular channel is not checked on an event by event basis, one ADC can serve multiple channels by means of analog multiplexing. The same time digitizer chip [2] is used by both the FEBs and the SFEs. The L1 buffers are read out by a DSP based readout controller on a custom high speed data bus using the J3 backplane. Each VME crate houses up to ten

SFE cards, the readout controller card, and a Motorola 680xx based VME processor to provide parameter downloading and testing.

The mini-drift tubes (MDT, 48,000 channels total) have their electronics located in 192-channel 9U VME cards. The mini-drift tube digitizing cards (MDC) perform a low resolution (18.8 ns/bin) measurement of the drift time, improving the coordinate resolution of the tubes to a few millimeters compared to the 10 mm tube diameter. The MDC also has a digital pipeline and L1 buffers to store event data. They also are read out by a specialized DSP based readout controller via the J3 backplane. The MDT crates can accommodate up to twelve MDCs, a readout controller and a VME processor to perform tasks similar to those of the scintillator system.

B. Trigger Architechture

The muon system must provide both L1 and L2 trigger information to the TFW (Figure 1) as opposed to some other D0 detectors which send trigger information only to L2. The muon L1 trigger system receives data from the various front-end systems and provides information every 132 ns to the TFW. Due to the distributed nature of the muon system there are a large number of L1 trigger inputs (over 150). The muon L1 Concentrator cards perform data compression and an initial stage of pattern recognition to reduce the data flow into the L1 trigger system to a reasonable level. The TFW analyzes trigger information and generates an L1 decision which is distributed via high speed serial links to the Geographic

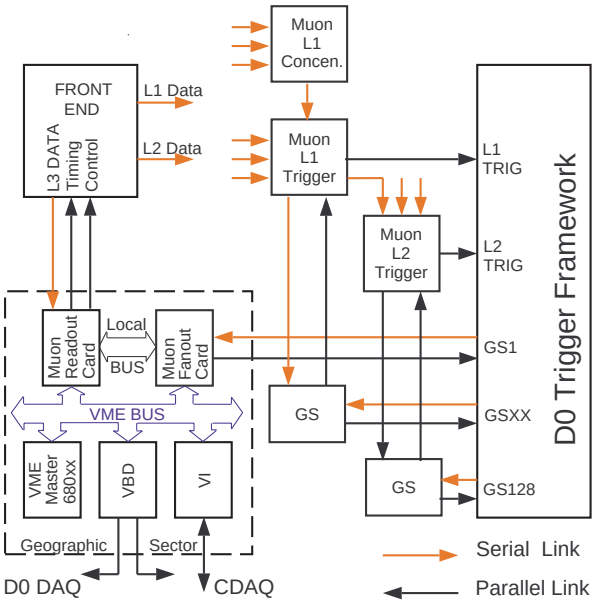

Figure 1: D0 muon trigger architecture. GS - geographic sector.

Sectors. The TFW attaches a unique trigger number to each L1 decision for event synchronization. This is discussed in more detail in the next section. Each muon front-end also provides L2 information to the Level 2 trigger system. Upon receiving an L1 accept, the front-ends not only buffer the event, they also send a portion of the event to the L2 trigger system via serial links.

A GS consists of a VME crate containing the D0 standard interface to the DAQ called the VME Buffer Driver (VBD) and a control and timing interface between the TFW and the front-ends connected to it. The front-end electronics and L1 trigger system are located on the D0 detector platform and connected to the readout crates by both twist and flat and ribbon coaxial cables. The Muon Fanout Card (MFC) distributes timing, control and trigger information by means of custom J2 connections on the crate backplane. It also receives status and error signals from the Muon Readout Cards (MRC) located in the crate and transfers this information back to the TFW.

The Muon Readout Card is an intermediate stage between the MFC and two front-ends. It sends timing, control and trigger information, and receives status and error signals from the front-ends. It also has internal memory for buffering one event. The MRC and MFC are the standard muon GS interface cards. The data transfers between the VBD and MRCs are initialized by the 680xx processor, which also performs trigger number checking and event header formatting. In local mode, it is used for diagnostics and local data taking and processing. The Vertical Interconnect (VI) is a part of the D0 slow control and monitoring system. It affords remote access to the crate VME address space.

C. Event Synchronization

A major concern for buffered data acquisition systems is synchronization of the data comprising the events. We propose to use several levels of checking to identify errors and simplify debugging. The structure proposed for colliding beams in the Tevatron consists of three superbunches separated by abort gaps. The beam crossing intervals may be 132 or 396 ns, but in either case, the TFW synchronization time unit will be 132 ns.

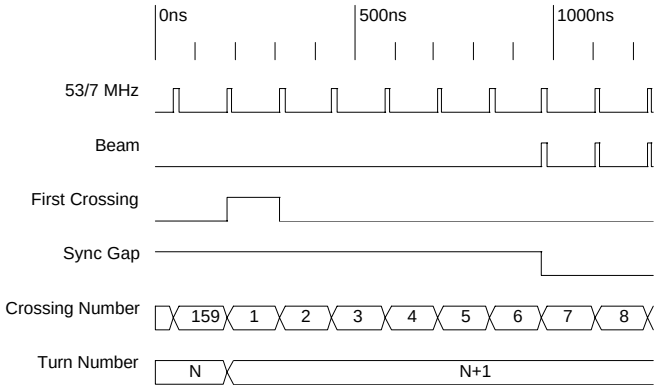

Figure 2: Timing diagram showing relevant signals at first crossing

Each front-end receives a copy of the Tevatron RF and a special reset signal (First Crossing, FC, Figure 2)

synchronized to it and arriving once per beam turn at a fixed offset from the beginning of the first collision in the superbunch. The clock and reset signals are used by the front-ends to run two counters which together provide a unique identifier for each collision. One eight bit counter is clocked at 53/7 MHz and generates a crossing number. This counter is preset to one at the start of each turn. A second counter, 16 bits wide, clocked by the FC signal, generates a turn number. These counter values are delayed and read out in the same manner as data. These two numbers are appended to events and are used by the data acquisition system for checks of event synchronization. In the muon system the crossing number simplifies the task of timing adjustment thus increasing system reliability. If there is no match between the crossing number emerging from the pipeline and the trigger number sent by the TFW, an error is generated.

A global initialization signal (INIT) is generated by the TFW to synchronize all sub-systems before data taking begins. An INIT Acknowledge (INACK) is returned by the GSs when they finish their local initialization. When all the GSs return INACK, the TFW releases INIT and begins issuing trigger decisions. This method of synchronization allows for rapid re-synchronization and quick detection of any sub-systems that fail to initialize properly.

III. Muon Readout

A. DSP Data Processing and Buffer Management

The D0 DAQ specification stipulates that all front-ends implement 16 L1 and eight L2 buffers to store events corresponding to the appropriate TFW decision (Figure 3).

Each GS is required to have a pipeline to store incoming events until a TFW decision is made. The minimum pipeline delay is determined by the Level 1 decision time of 3.56 μs (at the TFW location) and the signal propagation time from the TFW to the GS. Each GS must have the ability to store events accepted by the TFW. Events accepted by L1 and L2 decisions are stored in Level 1 and Level 2 buffers. L2 REJECT discards event from the Level 2 buffer. The muon system buffering scheme follows the D0 specification by implementing flexible DSP based control of the event buffering. A simplified diagram of the muon buffering scheme is shown in Figure 4.

A continuously running digitizer generates output information synchronously with the Tevatron RF. A digital pipeline delay, running synchronously with the digitizer is preset to the TFW Level 1 trigger decision time. When the L1 accept arrives at the front-end, corresponding event information appears at the delay output and is transferred to the L1 FIFO. After that, the event information can be asynchronously read out by the readout logic and stored in the intermediate L1 buffer within the DSP memory. From this point on, the DSP takes control of both processing and buffering.

The specified maximum for Run II is about 10 kHz for the L1 trigger rate and 1 kHz for L2. An average interval of 100 μs is thus available for transferring an event from the output

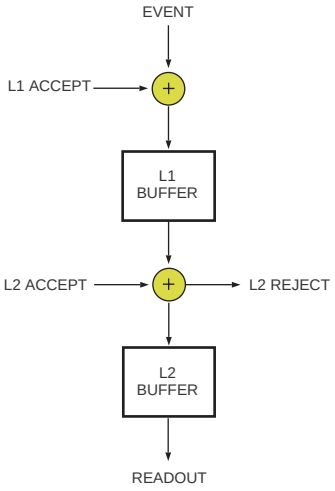

Figure 3: D0 buffering scheme.

of the delay to the L1 buffer. In the muon system this process takes about 1.5 μs maximum. This deadtime makes no contribution to the DAQ deadtime because, for other reasons, the minimum interval between Level 1 triggers is 2.6 μs.

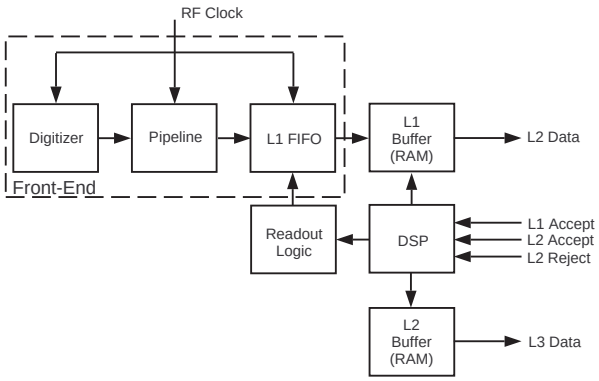

Figure 4: Muon system buffering scheme. DSP - digital signal processor.

The Analog Devices simulator for the ADSP-2181 processor has been used to estimate how long it will take to process and format the data before sending it to the MRC. Physics simulations of the Run II scenario show that the expected occupancies for the PDTs, scintillation counters and MDTs are 3%, 1% and 0.5% respectively. We use 10%, 10% and 1%, since accurate occupancy estimates are impossible without real background measurements.

For the PDT front-ends, assuming a 10% occupancy, the correction of the time scale, pedestal subtraction and gain correction will take about 12 μs. A calculation of pad

electrode charge ratios to determine the second coordinate will take about 8 μs. The time to readout and transfer an event to the MRC is estimated to be 9.1 μs and 6.2 μs respectively for a total of 35.3 μs or 3.5% of the average interval between two L2 accepts.

The event size for the scintillation counters is smaller than for the PDTs. The ten SFE cards that will be placed in one VME crate will produce about 30 16-bit words per event assuming 10% occupancy. This will take about 2.5 μs to readout, 15 μs to correct t_0 and convert bins to nanoseconds and 4.2 μs for the transfer to the MRC. Thus, total front-end data processing takes about 21.7 μs.

The MDC drift time data, which is not zero-suppressed, has an event size fixed at 216 32-bit words and is the largest of the three detector subsystems. The readout controller will sparsify and reformat the data into 16 bit form, a process estimated to take 9 μs. For the MDTs the average occupancy is expected to be in the range of 0.5% to 1%. Assuming 1% occupancy, the simulation shows that to convert bins to nanoseconds and to correct t_0 will take about 6.4 μs. The transfer time to the MRC is about 2.5 μs. The front-end data processing takes about 17.9 μs.

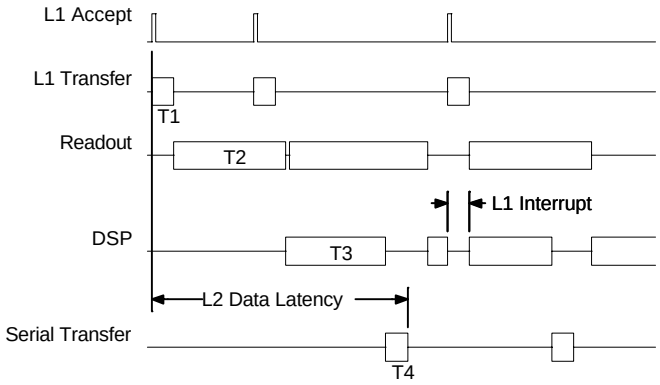

Figure 5: L2 data processing timing diagram. T1, T2, T3 and T4 correspond to the data processing times shown for one event.

The DSP also performs L2 data processing and formatting, which is time critical. Based on queuing simulation of the D0 data acquisition system [4], L2 data latency cannot exceed 30 μs without introducing additional dead time. The typical L2 processing times are shown in Figure 5. We have estimated that for conservative occupancies of 10%, 10% and 1% described above the following processing times can be achieved (Table 1).

For event buffer management, every trigger decision causes a DSP interrupt which is used to store information in a TFW decision FIFO (Figure 6). If there was an L1 accept, the DSP checks if the TFW crossing number corresponds to the local crossing number provided by the synchronization logic. In the case of a mismatch an Error 1 signal is generated. If there was an L2 accept or L2 reject, the DSP checks the corresponding number associated with the event stored in the L1 buffer. In this case, a mismatch generates an Error 2. The DSP also checks the status of its buffers and generates Busy 1 or Busy 2 signals when appropriate.

Table 1.
L2 data processing times in μs.

Detector	T1	T2	T3	T4	total
PDT @ 10%	4.5	12.0	12.0	3.0	31.5
SC @ 10%	0.6	20.0	7.0	5.4	33.0
MDT @ 1%	0.1	9.0	6.4	0.5	16.0

An event accepted by L1 is collected from the front-end L1 buffers by subsystem specific readout logic and written into the DSP memory. The DSP then processes and formats the data according to the requirements of the L2 trigger system. After processing, the data is sent to L2. An L2 accept causes the DSP to process the event according to the L3 system requirements, buffer the event and wait for permission to transfer it to the MRC card for final event building in the muon readout crate. An L2 reject discards the event, freeing up one L2 buffer. Our estimates show that all the necessary buffer management including interrupt handling can be done using the ADSP-2181 within 1.5 μs.

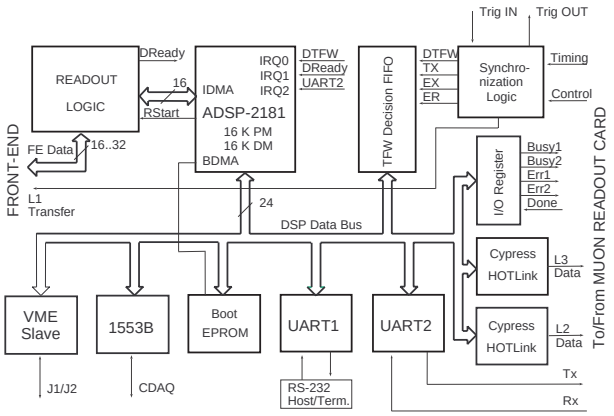

Figure 6: Muon Readout Controller. DTFW = L1 Accept + L2 Accept + L2 Reject, TX - TFW crossing number, EX - Event crossing number, ER - Event turn number.

As one can see, the processing times are within the required ranges and we conclude that using the DSP to perform these tasks will have a negligible impact on the D0 DAQ system deadtime.

B. Muon Readout Card

The Muon Readout Cards are located in the readout crates in the Movable Counting House. Each MRC has two independent identical sections (A and B) connected to two front-end units. A block diagram of the MRC is shown in Figure 7. The data is transferred from the front-end readout controller via copper coaxial cable using a Cypress HOTLink

chipset (CY7B923/933). We use its lowest frequency setting of 160 Mbit/s to accommodate our transmission line bandwidth. With 360 feet of coaxial cable we have achieved error free transmission using a passive cable compensation network. The MRC receives 16 timing and control signals from the Muon Fanout Card and transmits back five status signals.

Each MRC section includes an eight Kbyte dual port memory buffer for data storage, a 32 bit status/control register, a serial communication controller (SCC) to communicate with the DSP processor and transmitters and receivers for 20 control and timing signals in each section. A VME slave interface and transmitters and receivers for J2 backplane are common for both sections. 16 control signals are transmitted to and from the front-end readout controller using twist and flat cable. Three timing signals including Tevatron RF, reset and encoded gap signal, and serial data are transmitted on four coaxial cables. The typical length of these cables is 280 feet.

For the twist and flat cable, differential current drivers (SN75110As from Texas Instruments) are used at the

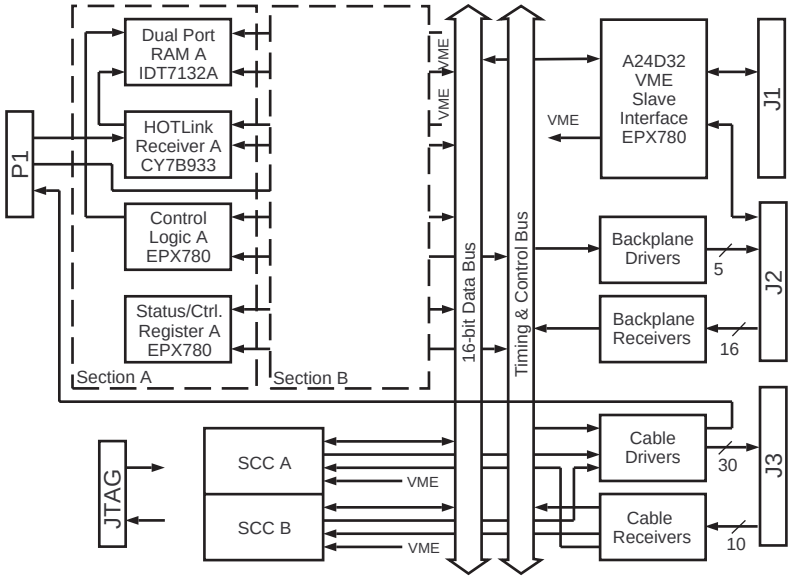

Figure 7: Muon Readout Card. VME - VME command, SCC - Serial Communication Controller.

transmitter end, and current feedback amplifiers (AD8002 from Analog Devices) and high speed comparators (MAX902 from Maxim) are used at the receiver end. The amplifiers have a feedback compensation adjusted for the cable attenuation. A Motorola MC10H116 in PECL (Positive ECL) mode is used on both ends for coaxial cable differential driver and receiver. To reject common mode voltages between the receivers and the transmitters, RF transformers are used to convert from differential to single ended at the transmit end and back at the receive end.

Two special control characters are used to indicate the beginning and end of the data transmission. A K28.0 character indicates beginning of the event and K27.3 character is the end of event data marker. These characters are used by the HOTLink control logic implemented in an ALTERA EPX780 FLASHLogic chip to initialize its address register and will not be stored. The HOTLink chips use K28.5 pad characters to keep the receiver synchronized with the transmitter and to align the incoming bit stream. The control logic ignores these characters which allows an intermittent byte stream at the transmitter end. There is a time-out counter preset to 4 ms to prevent ‘hanging’ of the link.

Event data from the HOTLink receiver is written into one port of the memory, while the second port is accessible to VME for both writes as well as reads. The status register includes busy and error signals coming from the front-end readout controller and a set of control and status bits. Busy 1, Busy 2, Error 1, Error 2 and the Service Request signals are wire ORed on five J2 backplane lines and transmitted to the MFC. Each of these signals may interrupt the VME processor using the interrupt controller in the MFC. The service request is the OR of internal interrupt sources which include the HOTLink control logic and the UARTs.

A Zilog Z16C30 Serial Communication Controller (SCC) is used to communicate with the DSP processors in the readout controllers. It provides a 1 Mbit/s data rate which has been tested using the cable connection described earlier. The SCC has two independent sections each of which uses two 16 bit access VME addresses.

C. Muon Fanout Card

The Muon Fanout Card is the interface between the TFW and the muon readout crate. The MFC receives timing, control and trigger information from the TFW via the Serial

Communication Link (SCL), and distributes it on J2 user defined lines. The SCL is a D0 standard interface daughter card which converts serial data to parallel. The MFC communicates with the TFW by sending Error 1, Busy 1, Error 2, Busy 2 and INACK. Error signals indicate error conditions associated with Level 1 or Level 2 activities. Busy signals indicate availability of the event buffers.

The TFW provides two types of accelerator gap signals for Geographic Sectors. One gap per beam turn is used by the L1 trigger system to synchronize its input FIFOs receiving data from the different front-end systems. This gap is called sync gap and during this interval, pad characters are sent to the L1 trigger system. The other two gaps can be used, for example, for pulsing the front-ends at a time it is known there will be no beam triggers. Because of the limited number of connections between the platform and the movable counting house, a scheme for encoding two signals onto one line is used for the gaps. The Tevatron RF is transferred unaltered on one coax to the readout controller. A phase locked loop is used there to remove jitter, and to restore duty cycle symmetry, a requirement of the TDC chips.

The MFC includes a VME A24D16 slave interface, FIFO memories for the beam crossing and turn numbers, an interrupt controller, a real time clock, three control/status registers, a timing sequencer and counters for TWF decisions. The MFC is controlled by the VME processor in the readout crate. Error 1, Error 2, Busy 1, Busy 2 from each MRC are wire OR'ed on J2. The OR of these backplane signals as well as INIT and L2 accept can interrupt the VME processor. To localize the interrupt source the processor reads status registers in the MFC and MRCs and calls the appropriate service routine. The block-diagram of the MFC is shown in Figure 8.

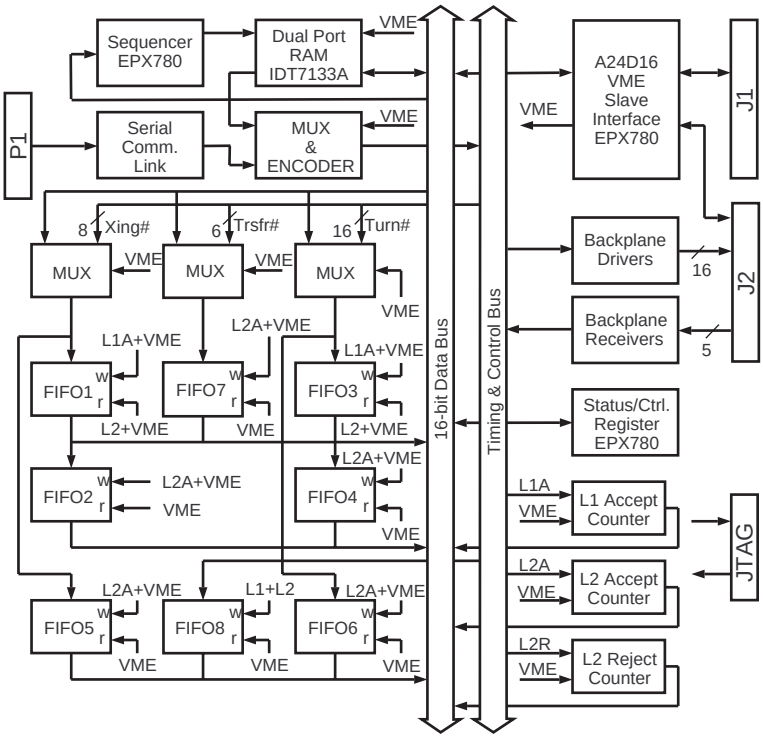

Figure 8: Muon Fanout Card. L1A - L1 accept, L2A - L2 accept, L2R - L2 reject, L2 = L2A + L2R, VME - VME command.

Each L1 or L2 TFW decision is uniquely identified by a specific crossing and turn number. All TFW decisions along with their trigger numbers are stored in FIFOs and transmitted to the front-ends via the MRCs. All the FIFOs are 256 deep which is much more than the 16 L1 buffers and eight L2 buffers required by the D0 DAQ specification. FIFO1, FIFO2 and FIFO3, FIFO4 are used to mirror the state of the front-end data buffers. Crossing numbers pass through FIFOs one, two and five, and turn numbers pass through FIFOs three, four and six.

For each L1 accept, an associated 8-bit beam crossing number is stored in FIFO1. At each L2 accept, a crossing number is moved from FIFO1 to FIFO2. At the same time, the crossing number issued by the TFW is stored in FIFO5. Sixteen bit beam turn numbers move through FIFOs three, four and six in a manner identical to the crossing numbers.

When the VME processor builds the event, it reads one word from FIFO2 and FIFO4 and compares these numbers with those from FIFO5 and FIFO6 which contain the trigger numbers corresponding to the most recent L2 accept. In this way, on a trigger by trigger basis, synchronization is checked.

FIFO8 is used to store a sequential record of all TFW decisions. The depth of the storage is fixed at 256 triggers. The record is readable by VME for diagnostic purposes. Three 12 bit counters for scaling TFW decisions provide an additional diagnostic.

In addition, the GS is required to append an L3 transfer number furnished by the TFW to event data (FIFO 7). These numbers are used by the D0 DAQ system for checking data consistency.

Because of the sequential order of the trigger decisions, checking event synchronization is relatively simple. The crossing and turn numbers associated with a given TFW L1 decision remain attached to an event while it passes through all trigger decision levels. In the muon system, the crossing number is transmitted to the front-ends and checking is performed by the front-end readout controllers, but the turn number is generated locally by the readout controllers and is attached to the events by the DSP. This number is verified by the VME processor during event building. If there is a mismatch between two turn numbers an Error 2 is generated.

The ability to run locally for the purposes of system installation and checkout has proven to be very important in Run I of D0. The MFC has the ability to emulate the SCL by means of an internal pattern generator based on a 2Kx16 dual port RAM. The sequencer can run in both single cycle and continuous mode. The RAM contents are loaded from the VME bus. Another important diagnostic feature is a real time clock. As required by the D0 DAQ specification, each error condition, initialization procedure and any system specific condition has to be recorded. All related information including trigger numbers and a time stamp are written as a record into a file containing the 16 most recent entries. This information has to be available to the standard D0 on-line tools like CDAQ.

Differential PECL drivers have been successfully tested for distribution of the time critical signals such as RF clock, FC and encoded gap signals. LVDS (Low Voltage Differential Signaling) drivers and receivers are presently being tested and may be used if they prove to be better than PECL. The rest of the signals use standard VME levels and terminations.

The MFC is fitted with a VME interrupter with the five inputs connected to the MRC wire OR lines and a sixth input for the initialization signal from the TFW.

IV. Conclusion

As of this writing, the initial designs for the FEB, MRC and MDC are complete. A prototype MRC has been built and tested. The CB, SFE, Scintillator Readout Controller and Mini-Drift tube Readout Controller are still in the design phase. Initial prototypes are expected to be completed in the first half of the coming year.

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